Mixed-signal integration requires good design practices

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Consumer end markets are driving higher levels of mixed-signal integration in semiconductor products in order to drive system costs down. At present, semiconductor companies are required to deliver complex mixed-mode SoCs (systems on chip) on time to unforgiving OEMs, or face being designed out of the product. To complicate matters, the environment in which mixed-signal circuits must co-exist with complex digital circuits is becoming even more hostile.

Traditionally, mixed-mode SoC designers plan at least one silicon respin. This is due to the risks involved in instantiating sensitive mixed-signal circuits onto less-than-ideal manufacturing processes in the presence of significant digital interference.

For consumer semiconductor markets where roadmaps are unpredictable, this is an increasingly unacceptable position because the design timelines will no longer tolerate such a respin. The challenge is pushed back to the designers to achieve a first-time-right result. Mixed-signal integration can be achieved through the following design, isolation, verification, validation and design methodology techniques.

Smart floorplanning

Critical mixed-signal circuitry should be a central consideration for SoC floorplanning. These components should be placed as close as possible to the related analog input, output and supply bond pads. The "quiet" digital blocks, such as memories, should be placed between the analog blocks and the noisy digital blocks in order to maximize their distance through the substrate, and thus attenuate digital noise coupling components.

Such a floorplanning strategy can impose severe timing constraints. Therefore, digital system performance limitations should be considered at the outset of the design process.

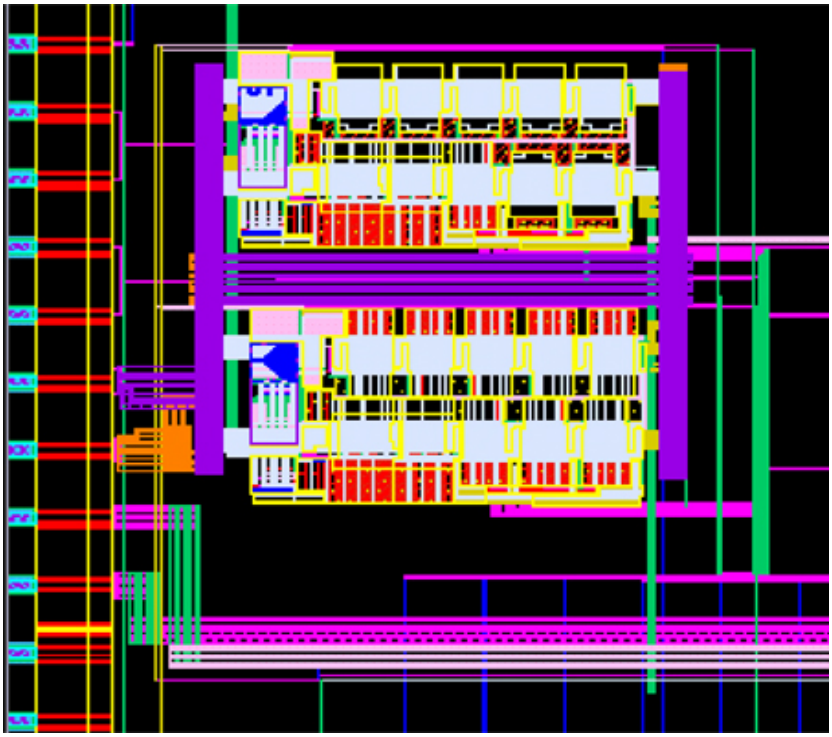

Figure 1: Placement is critical for mixed-signal circuits such as analog-to-digital converter (ADC) blocks.

Pad-ring design is critical

The pad-ring design is one of the most critical aspects of mixed-mode SoC design. Digital and analog I/O supply domains should be physically partitioned and electrically isolated from each other. However, the designer should be mindful of maintaining robust electrostatic discharge (ESD) performance, which may require the addition of level shifters between supply domains and the incorporation of local ESD protection.

Any integrated oscillator embedded in the pad-ring should have a dedicated power supply when providing a reference clock for data converters, mixers, sampling functions or PLLs. Otherwise I/O (input/output) related noise components will be mixed with the input signals of these functions, creating spurious output characteristics.

Output buffer slews should be carefully selected for minimum on-chip disturbance. Sensitive analog input and output pads should be kept away from noisy pads. Each analog I/O differential pad pair can be separated from noisier I/O signals by placing static or quiet bond pads on either side. The designer should place the analog power supply pads centrally in the pad-ring to minimize bond wire lengths and impedance in the supply path.

Substrate isolation

A key element of S3's isolation strategy is to minimize the number of active components in the substrate. Most modern deep sub-micron processes offer a deep-nwell option that has been shown to provide effective substrate isolation well into the gigahertz region. This deep-nwell should be placed under all digital logic with an nwell moat around the block perimeter to prevent digital noise contamination of the substrate.

If possible, the I/O components in the pad-ring should also be isolated from the substrate using deep-nwell for similar reasons. This strategy may require close co-operation with the standard cell, memory and I/O library vendors. We also recommend the placement of deep-nwell beneath sensitive mixed-signal circuits. This nwell region is connected to a quiet supply which will prevent residual substrate noise from coupling to the analog circuitry.

There is a cost associated with executing these isolation recommendations. The creation of these isolated pwell regions will add cost in the form of extra masks for the deep-nwell, and extra area for the nwell moats surrounding each region. In addition, extra supply pins may be required to create "quiet" nodes to ground these regions.

The implementation is quite complex. For example, the designer must be careful to ensure that a "quiet" region does not get inadvertently connected to a "noisy" domain in the pad-ring. So-called hot-nwell regions in analog circuits will get automatically connected to the deep-nwell beneath unless removed. These techniques are key to achieving successful first-time-right results that ramp rapidly to volume, comfortably mitigating the additional costs involved.

Regulator integration

By integrating linear regulators into the SoC, the designer can generate local "quiet" supplies for analog domains without the requirement for extra bond pads and package pins. This creates some flexibility and supports the isolation strategy.

For supplying noisy digital functions, on-chip regulation can help attenuate the large current spikes if used in conjunction with on-chip decoupling capacitance. By ensuring that these current spikes do not propagate directly through bond wires, high frequency supply oscillations (ringing) are prevented, which could otherwise couple through to sensitive analog circuits and create high frequency emissions from the IC.

Mixed-mode simulation

The integration of RF and mixed-signal circuits onto SoCs has enabled the use of increasingly complex digital/analog feedback loops. These loops are used to dynamically adapt the amplification and filtering settings according to the system input signal characteristics, which can vary dramatically, especially in communication systems. They are also used to calibrate the analog and RF circuitry, whose characteristics can vary significantly due to the inherent variability and increasingly hostile environment of the CMOS manufacturing processes.

By employing adaptive loops, the designer extracts the highest level of performance and flexibility from the analog portion of the SoC. However, the behavior of such closed loops can be difficult to predict, and the designer risks introducing instability. Full mixed-mode system level modeling and simulation can be employed to mitigate these risks by accurately testing the behavior of the system.

It is important that such a modeling capability is introduced into the project at a very early stage in order to capture behavioral and architectural design problems in time to be fixed. The designers should develop an analog/mixed-signal model for each of the RF/analog functional blocks in the system during the specification phase of the project. System C models can be used to quickly prototype digital functionality.

The latest mixed-mode behavioral simulation tools from the leading EDA vendors allow efficient simulation of these combined domains with high resolution time stepping (for GHz RF systems) over meaningful simulation intervals in a matter of hours, even for very complex systems. This allows behavioral, polarity and functionality problems to be detected at an early stage of the design process, preventing a significant bug hunting and fixing effort. Later, during the IC implementation phase, schematic and RTL simulations are used to calibrate the original behavioral models to confirm their accuracy.

IP minimizes risk

If it’s not broken, don’t fix it and don’t re-invent the wheel. One of the key drivers of the emerging commercial mixed-signal intellectual property (IP) market is risk mitigation. For sure, the IP user benefits from the inherent cost savings that using IP provides compared to designing the component from scratch. The real value proposition for mixed-signal IP, however, is in the tangible benefit of reduced mixed-mode SoC design risk.

The user should identify the mixed-signal IP component which most closely matches his/her requirement, certify that the IP has met the stated performance in silicon/production, and integrate the component into the SoC without modification wherever possible. This last point is important – once a modification is made to the IP, the connection to its silicon proven status is severed and the inherent value is diminished.

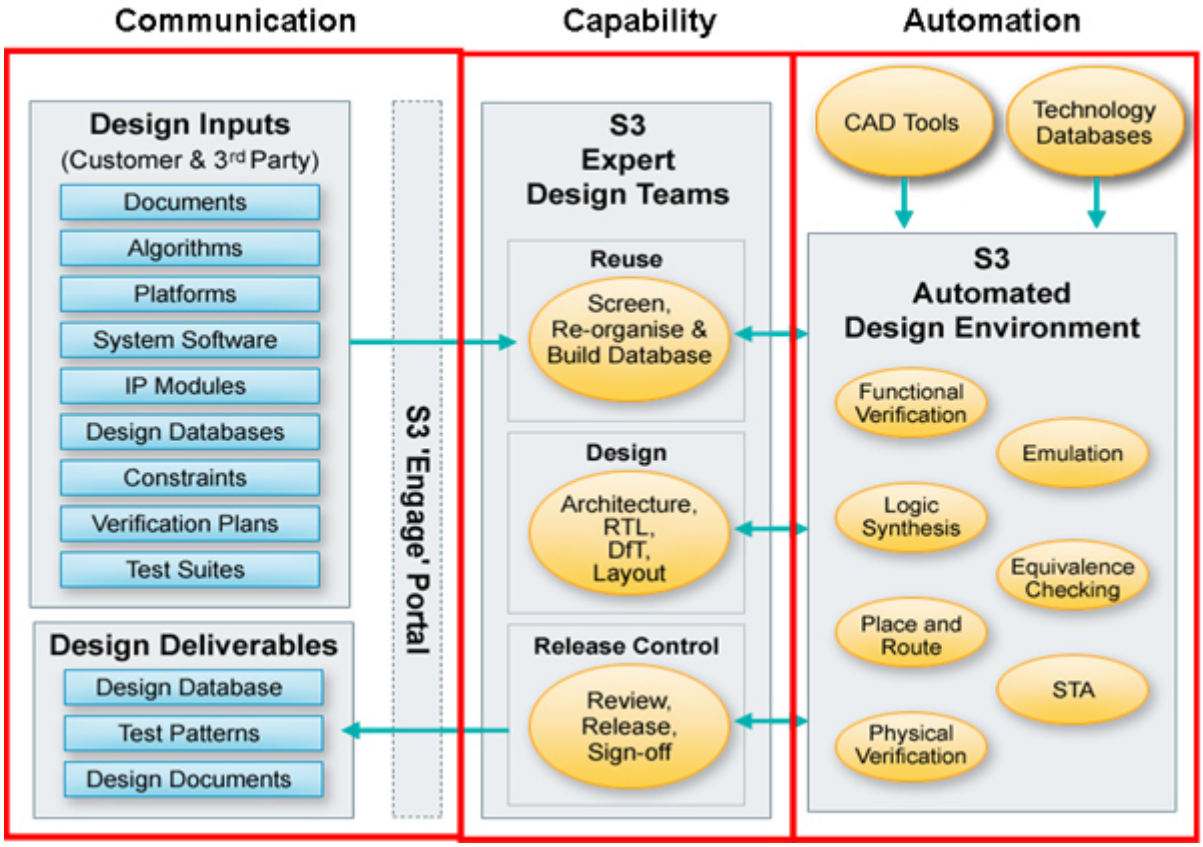

Figure 2: The mixed-signal IP selection and development process.

Test chips

At the circuit design level, transistor-level simulation models are becoming more accurate within a well-defined environment. However, as process scaling extends to 90 nm and 65 nm, the performance of the transistor is increasingly affected by its physical environment and its proximity to other devices. Such effects are not adequately captured by extraction and simulation tools, so the measured silicon results may be significantly different from those achieved by simulation.

Therefore, a dedicated test chip should be considered part of a risk mitigation strategy. New mixed-signal circuits at advanced technology nodes or major modifications to existing mixed-signal IP require such a test run. This is facilitated by foundry multi-project wafer runs. Those high performance mixed-signal components should be identified at an early stage of the development, as they will lie in the overall critical path. The specification and implementation of these circuits should be given the highest priority to allow time for their independent validation on silicon before integration with the rest of the system.

In summary, mixed-signal integration is becoming more prevalent in consumer electronics systems, driven primarily by cost reduction. But designing mixed mode SoCs become more

difficult at leading process geometries, and the risk of missing aggressive time to market deadlines has never been greater.

A design methodology with risk reduction at its core is of the utmost importance to competing successfully in the consumer semiconductor marketplace. Ultimately, experience is key. Ensuring your design team has a deep understanding of these issues will be critical to the success of your business – after all, you only get one chance to get it right the first time.

References

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